Remarks

Reconsideration of the application is requested. Please call the undersigned to discuss this case after consideration of the following points.

Claim 1 recites "A programmable logic device comprising: ... non-volatile memory adapted to store data which is transferable to the volatile memory to configure the programmable logic device;..." Similar limitations appear in independent claims 12, 18, 25, and 31. Applicants submit that Fox does not show or describe this structure, for at least the following reasons:

- In Fox, non-volatile memory 203 within CSoC 101 is conventional boot memory adapted to store initialization code for CPU 26 – not configuration data for CSL 201. See col. 4, lines 49-58. Furthermore, there is nothing in Fox to suggest that what is stored in internal non-volatile memory 203 is ever transferred to non-volatile memory in CSL 201. Rather, the stored initialization code is transferred from non-volatile memory 203 only to CPU 26.
- Nowhere does Fox unambiguously describe the transfer of configuration data from non-volatile memory 203 to CSL 201. Such a description would be present if Fox indeed disclosed such a transfer.
- In contrast, Fox clearly describes the conventional approach of using external non-volatile memory for storing configuration data for internal volatile configuration memory. He states this in a number of places such as at col. 4, lines 26-30: "A memory interface unit (MIU) 204 facilitates the transfer of logic values for the configuration memory cells from an external memory (for example, memory device 103 (FIG. 1)) to CSL 201 via a system bus 205."
- Fox strongly implies at col. 5, lines 6-10 that only an external memory device can supply configuration data to CSoC 101: "If memory device 103 is disconnected, then CSoC 101 must have been previously programmed, i.e., all values already loaded into the configuration memory cells [of CSL 201], and a reset function triggered." This statement makes sense only if internal non-volatile memory 203 is

incapable of supplying configuration data to the configuration memory cells of CSL 201.

Claim 1 further recites "a second data port adapted to receive external data for transfer into either the volatile memory or the non-volatile memory." Similar limitations appear in claims 12 and 18. Applicants submit that Tsui does not show or describe this structure, for at least the following reasons:

- Tsui discloses a first data port (e.g., JTAG port 108 in Fig. 1) that is adapted to receive external data for transfer into either the internal volatile memory or the internal non-volatile memory. The second data port (e.g., CPU port 110) is not so adapted. See, for example, col. 3, lines 12-24 and lines 54-60.
- This arrangement of data ports is also seen in Fig. 3, with first data port 302 adapted to receive external data for transfer into either the SRAM 308 or EEPROM 306 and second data port 304 302 adapted to receive external data for transfer SRAM 308.
- What the Examiner identifies as first and second data ports in Fig. 2 are in fact the same (first) JTAG port, not different ports. The second data port in Fig. 2, as in Fig. 1, is a CPU port.

Claim 25 recites "A programmable logic device comprising: ... a CPU port adapted to receive external data for transfer into either the volatile memory or the non-volatile memory." A similar limitation appears in claim 31. Applicants submit that Tsui does not show or describe this structure, for at least the following reasons:

- The CPU port in Tsui (e.g., CPU port 110 in Fig. 1) is not adapted to receive external data for transfer into either the internal volatile memory or the internal non-volatile memory. See, for example, col. 3, lines 12-24 and lines 54-60.

Respectfully submitted,

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